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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/652,694	08/31/2000	Paul S. Gryskiewicz	INTL-0447-US (P9445)	3816

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EXAMINER

YENKE, BRIAN P

ART UNIT	PAPER NUMBER
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2614

DATE MAILED: 06/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/652,694

Applicant(s)

GRYSKIEWICZ, PAUL S.

Examiner

BRIAN P. YENKE

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on Amendment (31 March 2003).
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other:

**DETAILED ACTION**

1. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh et al., US 6,411,334 in view of May, US 5,815,168.

In considering claims 1 and 16,

a) *the claimed scaling a first portion and a second portion of image information to provide a scaled first portion and a scaled second portion...* is met where filtering unit 330, <sup>FIG 34</sup> which horizontally scales/filters (332/334) and vertically scales/filters (336/338) where memory buffer 240 stores the temporary data in properly sized buffers (col 4, line 6-8). Thus the unscaled portion if stored in a properly sized buffer would substantially fill a memory area.

However, Yeh does not specifically disclose storing the scaled first portion and scaled second portion in the first memory area, where the unscaled portion would fill the first memory area.

Yeh discloses an aspect ratio correction using digital filtering which scales a source array of pixel data in a memory by a scale factor to a destination array of pixel data.

It is also known that if data is scaled down (i.e. 2 to 1), only half of the original pixel information would be retained, thus reducing the size of the memory row used (applicant's drawings Fig 4b-c).

The storing of more than one scan line (row) onto a single row of memory is notoriously well known in the art.

The examiner incorporates May, US 5,815,168 which discloses in the background that it is well known to store two scan lines of data on one row of memory (Fig 2b). May then discloses a memory system which stores data in a tiled format in a display memory, where the parameters (tile size, tile height and tile width) may be altered in response to the video mode (e.g. pixel resolutions, pixel depth or the like) (col 9, line 51-62).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Yeh, which discloses scaling data both horizontally and vertically, by storing the scaled horizontal (first portion) and scaled vertical portion (second portion) in the first memory area, with May, in order to utilize the available memory, where a signal which is reduced (scaled down both horizontally and vertically,

i.e. 2-to-1) would be able to be stored in the first memory area which stored the unscaled horizontal signal, by storing the reduced/scaled two rows on the original row of memory unscaled, thereby efficiently using the available rows of memory.

In considering claims 2 and 17,

*a) the claimed accessing the first or second portion...* is met by graphics processor 210 of display processor 180 (Fig 2) which receives scaled data both from memory 240 and via pre-processing unit 320 (via memory interface 220).

*b) the claimed retrieving a data sample...* is met by filtering unit 330 which receives coefficients from memory buffer 240 and pixel data from pre-processing unit 320 (via memory interface 220).

*c) the claimed using the data sample in a second scaling operation* is met where the data is first scaled horizontally then vertically (Fig 3b).

In considering claims 3 and 18,

*a) the claimed dividing a memory into a plurality of lines* is met by graphics processor 210, which scales the array to a desired destination array of pixel data.

*b) the claimed identifying a line* is met by graphics processor 210 (Fig 3a)

*c) the claimed storing a number of scaled portions in the line...* is met by graphics processor 210 which stores the scaled portions (using filtering unit 330) into memory buffer 240 (Fig 2).

In considering claims 4-6 and 15,

*a) the claimed a memory...* is met by memory buffer 240

*b) the claimed scaling a first portion and a second portion of image information to provide a scaled first portion and a scaled second portion...* is met where filtering unit 330, which horizontally scales/filters (332/334) and vertically scales/filters (336/338) where memory buffer 240 stores the temporary data in properly sized buffers (col 4, line 6-8). Thus the unscaled portion if stored in a properly sized buffer would substantially fill a memory area.

*c) the claimed a memory controller coupled to the memory* is met by graphics processor 210 (Fig 2).

However, Yeh does not specifically disclose storing the scaled first portion and scaled second portion in the first memory area, where the unscaled portion would fill the first memory area.

Yeh discloses an aspect ratio correction using digital filtering which scales a source array of pixel data in a memory by a scale factor to a destination array of pixel data.

It is also known that if data is scaled down (i.e. 2 to 1), only half of the original pixel information would be retained, thus reducing the size of the memory row used (applicant's drawings Fig 4b-c).

The storing of more than one scan line (row) onto a single row of memory is notoriously well known in the art.

The examiner incorporates May, US 5,815,168 which discloses in the

background that it is well known to store two scan lines of data on one row of memory (Fig 2b). May then discloses a memory system which stores data in a tiled format in a display memory, where the parameters (tile size, tile height and tile width) may be altered in response to the video mode (e.g. pixel resolutions, pixel depth or the like) (col 9, line 51-62).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Yeh, which discloses scaling data both horizontally and vertically, by storing the scaled horizontal (first portion) and scaled vertical portion (second portion) in the first memory area, with May, in order to utilize the available memory, where a signal which is reduced (scaled down both horizontally and vertically, i.e. 2-to-1) would be able to be stored in the first memory area which stored the unscaled horizontal signal, by storing the reduced/scaled two rows on the original row of memory unscaled, thereby efficiently using the available rows of memory.

In considering claim 7,

*The claimed wherein the number of bytes in the memory is smaller than the predetermined number of bytes* is met where if the received video data stream is to be displayed on a correspondingly smaller destination display screen (302), the required memory in a decimation operation would be smaller.

In considering claim 8,

*The claimed wherein the scaling operation is a horizontal scaling operation* is met by horizontal filter 1 (332) and horizontal filter 2 (334) Fig 3b.

In considering claims 9-11,

*The claimed wherein a second scaler to perform a second scaling operation* is met by vertical filter 1 (336) and vertical filter 2 (338) which perform a scaling operation on the columns of data.

In considering claims 12-13,

Yeh discloses using digital filtering using horizontal and vertical filters/scalers which correct for an aspect ratio of a display by scaling a source array of pixel data in a memory by a scale factor to a destination array of pixel data.

However, Yeh remains silent on the scalers including a finite impulse response filter (FIR) with a look-up table.

Yeh does disclose that the horizontal coefficients (Fig 4) are processed/loaded into coefficient unit 410 (Fig 4) and the vertical coefficients are processed by vertical coefficient registers 1010-1012 (Fig 10), where the coefficients are both received from memory buffer 240.

A FIR filter is a type of digital filter, which has a finite impulse response, since there is no feedback in the filter. FIR filters are known to be "linear phase", which delay the input signal, but do not distort its phase. In addition, FIR filters are used in interpolation and decimation operations since the FIR filters allow some of the calculations to be omitted, thus providing efficiency in computing operations.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify/utilize a FIR filter, with Yeh, which discloses scaling



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source array of pixel data in a memory, where the arrays are scaled both horizontally and vertically, by using a FIR filter, in order to provide an efficient linear phase interpolation/decimation operation.

In considering claim 14,

The examiner takes "OFFICIAL NOTICE" in regards to a First-in-First Out Memory. Yeh et al., discloses a memory uses a memory buffer (240) , to correct the aspect ratio of a display by scaling the source array of pixel data in memory by a scale factor to a destination array of pixel data.

A FIFO memory, is a conventional device which exits the item/data from the system which has been in the system the longest. Thus data that has arrived subsequently to previous data, will be exited/output subsequently to the previous data as well.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify/utilize a FIFO memory architecture with Yeh, which discloses the changing/scaling the source array of pixels in a memory, by reading/writing data in and out of the memory in the order the data was received, to thereby maintain the integrity of the original data.

***Conclusion***

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Yenke whose telephone number is (703) 305-9871. The examiner work schedule is Monday-Thursday, 0730-1830 hrs.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, John W. Miller, can be reached at (703) 305-4795.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

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Washington, D.C. 20231

**or faxed to:**

**(703) 872-9314**

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703)305-4700.

B.P.Y.

23 May 2003



**JOHN MILLER**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2600**

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